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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

re Application of: James M. Thommes
Serial No. : 10/774128
Filing Date : February 5, 2004
For : Method And Apparatus For Receiving A
Universal Input Voltage In A Welding
Power Source

Attorney Docket No. : ITW 7188.64

Disclosure of Prior Art, Litigation, and Litigation Documents

Honorable Commissioner of
Patents and Trademarks
Washington, D. C. 20231

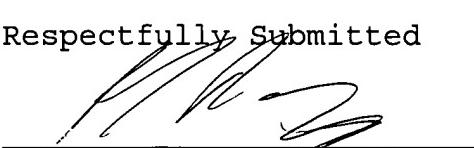
Dear Sir:

Enclosed is a form 1449 and cited art.

Also, pursuant to MPEP 2001.06(c) Applicant is hereby notifying the Office that at least some of the subject matter being claimed is the subject of an existing litigation (Case No. 1:03-CV-00966, ED Wis), wherein the assignee Illinois Tool Works Inc. has sued Thermal Dynamics Corporation. Applicant is including copies of papers from that litigation, including:

Defendant's Answer
Defendant's Amended Answer
Defendant's Answer to the Second Amended Complaint
Defendant's Answer to the First Set of Interrogatories
Defendant's Supplemental Answer to the 1st Interrogatories
These documents are being provided because the Defendant has asserted the parent patents are invalid. The prior art referred to by the Defendant has previously been cited, or is cited herein.

Respectfully Submitted


George R. Corrigan, Reg. No. 34,803
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Appleton, WI 54915
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PATENT

Attorney's Docket No. ITW 7188.64

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of : James M. Thommes

Application No.: 10/774128

Group Art Unit: 2838

Filed: February 5, 2004

For: Method And Apparatus For Receiving A Universal Input Voltage
In A Welding Power Source

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

TRANSMITTAL OF INFORMATION DISCLOSURE
STATEMENT BEFORE MAILING DATE OF EITHER
A FINAL ACTION OR A NOTICE OF ALLOWANCE

TIME OF TRANSMITTAL OF ACCOMPANYING
INFORMATION DISCLOSURE STATEMENT

1. The information disclosure statement transmitted herewith is being filed **after** three months of the filing date of this national application or the date of entry of the national stage as set forth in § 1.491 in an international application or after the mailing date of the first Office action on the merits, whichever event occurred last but before the mailing date of either:
 - (1) a final action under Section 1.113 or
 - (2) a notice of allowance under Section 1.311, whichever occurs first.

CERTIFICATE OF MAILING/TRANSMISSION (37 CFR 1.8a)

I hereby certify that this correspondence is, on the date shown below, being:

deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to the Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450.

Date:

12/22/04

George R. Corrigan

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180.00 OP

CERTIFICATION OR FEE

2. Accompanying this transmittal is the fee set forth in 37 C.F.R. 1.17(p) for submission of an information disclosure statement under Section 1.97(c). s (\$180.00).

FEE PAYMENT

3. Applicant elects the option to pay the fee set forth in 37 C.F.R. 1.17(p) for submission of an information disclosure statement under Section 1.97(c) (\$180.00).

Fee due = \$ 180.00

METHOD OF PAYMENT OF FEE

4. Please charge the fee of 180.00 and any additional fees that may be due, to the credit card specified on the attached sheet.



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Form PTO-1449 U.S. Department of Commerce Patent And Trademark Office					ATTY. DOCKET NO. ITW 7188.64	SERIAL NO. 10/774128	
SUPPLEMENTAL INFORMATION DISCLOSURE CITATION					APPLICANT James M. Thommes		
					FILING DATE February 5, 2004	GROUP 2838	
U. S. PATENT DOCUMENTS							
EXAM. INIT.	REF	PATENT NUMBER	DATE	NAME	CLASS	SUB- CLASS	FILING DATE
FOREIGN PATENT DOCUMENTS							
EXAM. INIT	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB- CLASS	TRANSLATION YES NO
OTHER DOCUMENTS (Including Author, Title, Date, Pages, Etc.)							
		Reduction of Voltage Stress in Integrated High-Quality Rectifier-Regulators by Variable-Frequency Control, M.M. Jovanovic, D.M. Tsang, and F.C. Lee, Proceeding of the Applied Power Electronics Conference, Orlando, FL, Feb. 13-17, 1994					
		Single-Stage Single-Phase Parallel Power Factor Correction Scheme, Y. Jiang and F.C. Lee, Proceedings of the Power Electronics Specialist Conference, Taipei, Taiwan June 20-25, 1994					
		A Novel Single-Phase Power Factor Correction Scheme, Y.M. Jiang, F.C. Lee, G.C. Hua, and W. Tang, Proceedings of the Applied Power Electronics Conference, San Diego, CA 3/7-11/93					
		Boost Power Factor Corrector Design With The UC3853, By Phillip C. Todd, Unitrode Corporation					
		A High Performance Linear Regulator For Low Dropout Applications, Dave Zendzian, Unitrode Corporation					
EXAMINER			DATE CONSIDERED				
EXAMINER: Initial if citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							

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FOREIGN PATENT DOCUMENTS								
EXAM INIT	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB- CLASS	TRANSLATION	
							YES	NO
OTHER DOCUMENTS (Including Author, Title, Date, Pages, Etc.)								
		Power Factor Correction Using The UC3852 Controlled On-Time Zero Current Switching Technique, Bill Andreycak, Unitrotode						
		UC3854 Controlled Power Factor Correction Circuit Design, Philip C. Todd, Unitrotode						
EXAMINER			DATE CONSIDERED					
EXAMINER: Initial if citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.								

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